

Honeywell's Docket No. H0003369 DIV (4960)
Practitioner's Docket No. 100665.0053US2



1732
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Jesse PEDIGO, et al.**

Group No.: **1732**

Application No.: **10/040,118**

Examiner: **Not Yet Assigned**

Filed: **January 3, 2002**

For: **Hole Filling Using an Etched Hole-Fill Stand-Off**

Box DD

**Assistant Commissioner for Patents
Washington, D.C. 20231**

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**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
WITHIN THREE MONTHS OF FILING OR
BEFORE MAILING OF FIRST OFFICE ACTION (37 C.F.R. 1.97(b))**

**IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING
INFORMATION DISCLOSURE STATEMENT**

The information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever event occurs last. 37 C.F.R. 1.97(b).

Respectfully submitted,

Date: April 11, 2002

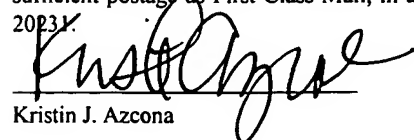
By: 

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Reg. No. 45,258

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CERTIFICATE OF MAILING (37 C.F.R. 1.8(a))

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.


Kristin J. Azcona

Date: April 11, 2002

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INFORMATION DISCLOSURE STATEMENT

Box DD
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure imposed by 37 C.F.R. § 1.56 to inform the United States Patent and Trademark Office of all references coming to the attention of the Applicant(s) or attorneys or agents for Applicant(s) which are or may be material to the examination of the subject application, attorneys for the Applicant(s) hereby invite the Examiner's attention to the references listed in the accompanying PTO Form 1449 entitled "List of References Cited".

This submission is understood to complement the results of the Examiner's own independent search. The submission of this Disclosure Statement should not be construed as a representation that a search was made, or that the cited items are inclusive of all relevant and material citations that may be available publicly.

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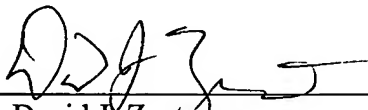
Applicant(s) respectfully request that the Examiner review the foregoing references, as set forth in the Form PTO-1449, and that they be made of record in the file history of the above-captioned application.

Respectfully submitted,

Rutan & Tucker, LLP

Dated: April 11, 2002

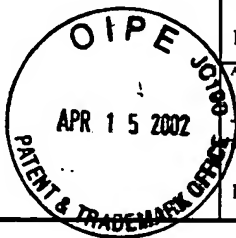
By: _____


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LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)



ATTY. DOCKET NO.

100665.0053US2

SERIAL NO.

10/040,118

APPLICANT

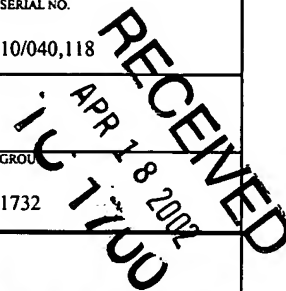
Jesse Pedigo, et al.

FILING DATE

12/20/01

GROUP

1732



U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,945,313	07/31/90	Synchronous Demodulator Having Automatically Tuned Band-Pass Filter	329	349	06/05/89
	5,117,069	05/26/92	Circuit Board Fabrication	174	261	09/28/90
	5,277,854	01/11/94	Methods and Apparatus for Making Grids from Fibers	264	86	06/06/91
	5,332,439	07/26/94	Screen Printing Apparatus for Filling Through-Holes in Circuit Board with Paste	118	213	08/18/92
	5,456,004	10/10/95	Anisotropic Interconnect Methodology for Cost Effective Manufacture of High Density Printed Circuit Boards	29	852	01/04/94
	5,471,091	11/28/95	Techniques for Via Formation and Filling	257	752	08/26/91
	5,532,516	07/02/96	Techniques for Via Formation and Filling	257	752	03/28/95
	5,610,103	03/11/97	Ultrasonic Wave Assisted Contact Hole Filling	437	225	12/12/95
	5,707,575	01/13/98	Method for Filling Vias in Ceramic Substrates with Composite Metallic Paste	264	104	07/28/94
	6,015,520	01/18/00	Method for Filling Holes in Printed Wiring Boards	264	104	05/15/97
	6,149,857	11/21/00	Method of Making Films and Coatings Having Anisotropic Conductive Pathways Therein	264	429	12/22/98
	6,184,133	02/06/01	Method of Forming an Assembly Board with Insulator Filled Through Holes	438	667	02/18/00
	6,261,501	07/17/01	Resin Sealing Method for a Semiconductor Device	264	272.15	01/22/99

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED